formal drawings and removal of the objections on form PTO-948 is respectfully requested.

Applicant thanks the Examiner for acknowledging his claim for priority under 35 USC §119. The certified copy of the priority document is filed herewith. Acknowledgement of receipt of the certified copy is respectfully requested.

Claims 4 and 6-10 are in this application. For the following reasons, it is respectfully submitted that these claims patentably distinguish over the prior art and are otherwise in condition for allowance.

Claims 1-3, 6 and 7 have been rejected under 35 USC §112 (second paragraph) as being indefinite. Claims 1-3 have been cancelled without prejudice or disclaimer, and replaced with new claims 8-10 while claims 4, 6 and 7 have been amended to more particularly point out and distinctly claim applicant's invention. It is therefore requested that the 35 USC §112 (second paragraph) rejection be withdrawn.

Claims 1-7 have been rejected under 35 USC §103 as unpatentable over McElroy. This rejection is respectfully traversed. For the following reasons, it is submitted that the invention of the application as disclosed and claimed patentably distinguishes over the McElroy reference.

Applicant's invention is directed to an improved semiconductor memory device, a significant feature of which is

that the memory cells, arranged in a matrix array of rows and columns, are divided into a peripheral group of memory cells and an internal group of memory cells, the internal group of memory cells being surrounded by the peripheral group of memory cells. Only the internal group of memory cells is connected to selection circuitry. Thus, selective access can be had to only memory cells of the internal group of memory cells. As the peripheral group of memory cells is not connected to the selection circuitry, none of the cells of the peripheral group of memory cells can be addressed through the selection circuitry.

Accordingly, the memory cells which are actually accessed by the selection circuitry are those memory cells of the internal group. None of the memory cells of the internal group face a region having no memory cells (i.e., a region outside the memory array). Rather, each memory cell of the internal group is surrounded by the other memory cells. They may be surrounded by other memory cells of the internal group or by other memory cells of the internal group and of the peripheral group. As explained in the specification at page 2, line 19 - page 3, line 14, memory cells of the internal group are formed with high uniformity and good electrical characteristics and therefore only the internal group of memory cells are used as functional memory cells to be accessed by the selection circuitry.

More particularly, there is regularity of layout in the internal group of memory because additional memory cells are necessarily arranged along all the peripheries of the memory cells of the internal group of memory cells. Therefore, for the memory cells of the internal group impurity diffusion is uniform to obtain a superior memory cell with uniform electrical properties. To the contrary, if at least one periphery of an array of the internal memory cells is not surrounded by the additional memory cells to expose an outermost memory cell of the internal memory group to a region having no memory cells, such outermost memory cells is likely to have different properties from those memory cells which are completely surrounded by other memory cells.

Thus, according to the teachings of the present invention, only memory cells of the internal group are used as functional memory cells to be accessed during addressing operations. Therefore, the memory device of the present invention is improved and has uniform characteristics over all addressable memory cells.

Such an improved semiconductor device is neither taught nor remotely suggested in the McElroy reference. Indeed, the teachings of the McElroy reference are entirely irrelevant to the teachings of the present invention. McElroy merely teaches an example of the memory cell array having redundant structure to

replace inoperative memory cells. In the McElroy memory, (see Fig. 1) redundant rows of memory cells 26A and 26B are provided for the memory arrays 10a and 10b respectively. The redundant row 26A or 26B is selected by a circuit 28A or 28B in place of a faulty row in the array 10a or 10b. The circuit 28A or 28B may form a part of a selection circuit which selectively accesses the memory arrays with the redundant rows. It is apparent that the memory cells of the redundant rows are actually accessed by the selection circuitry in place of faulty cells in the array 10a or 10b.

It should be noted that in the McElroy memory, memory cells along the three peripheries of each array 10a, (10b) are actually accessed. Therefore, the electrical characteristics of those memory cells arranged along the above three peripheries are inferior to those of the memory cells of the interior portion of the array 10a (10b). Thus, uniformity of memory cell characteristics cannot be obtained over all the addressable memory cells in the McElroy memory.

Quite clearly there is no teaching or suggestion in McElroy of providing two groups of memory cells, an internal group and a peripheral group of memory cells, the peripheral group of memory cells completely surrounding the internal group of memory cells such that each memory cell of the internal group is surrounded by

another memory cell, with only the memory cells of the internal group being selectively addressed by the selection circuitry.

In view of the foregoing, is respectfully submitted that independent claims 4 and 8 and their respective dependent claims 6, 7, and 9, 10 patentably distinguish over the prior art and are otherwise in condition for allowance. It is therefore respectfully requested that the application be passed to issue at the earliest possible time.

If the Examiner finds this application other than in condition for allowance he may wish to call the undersigned attorney at the local exchange listed below to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted

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